



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,737	12/14/2001	Kazuaki Ano	TI-33183	8828

23494 7590 05/23/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER

LEWIS, MONICA

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED

MAY 23 2006

GROUP 2800

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/017,737
Filing Date: December 14, 2001
Appellant(s): ANO, KAZUAKI

W. Daniel Swayze, Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 17, 2006 appealing from the Office action mailed May 18, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

No amendment after final has been filed. A response after final rejection was filed on September 16, 2005 amending no claims and requesting reconsideration of the final rejection.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20030038355

Derderian

2-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3-5, 7, 8, 10, 21, 23-26 and 28-30 are rejected under 35 U.S.C. 102(a) as being anticipated by Derderian (U.S. Publication No. 2003/0038355).

In regards to claim 1, Derderian discloses the following:

a) a first chip (10) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (For Example: See Figure 9); and

b) a second chip (110) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (For Example: See Figure 9);

c) a first attach layer (115) having an area equal to an area of said second chip bottom surface for directly coupling said first chip and said second chip, said first attach layer having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip (For Example: See Figure 9); and

d) a second attach layer (116) having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness and cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip (For Example: See Figure 9).

In regards to claim 3, Derderian discloses the following:

a) first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond (For Example: See Figure 9 and Paragraphs 62 and 63).

Art Unit: 2822

In regards to claim 4, Derderian discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas (For Example: See Figure 9).

In regards to claim 5, Derderian discloses the following:

a) first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip (For Example: See Figure 9).

In regards to claim 7, Derderian disclose the following:

a) first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond and said second attach layer is silicon dioxide (For Example: See Figure 9 and Paragraphs 62 and 63).

In regards to claim 8, Derderian discloses the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness (For Example: See Figure 9).

In regards to claim 10, Derderian discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip (For Example: See Figure 9).

In regards to claim 21, Derderian discloses the following:

a) a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface (For Example: See Figure 9);

b) a wire having a bond to one of said first bonding pads (For Example: See Figure 9);

c) a second chip having opposing top and bottom surfaces and positioned with said bottom surface adjacent said top surface of said first chip (See Figure 9);

d) a first attach layer to directly couple said top surface of said first chip and said bottom surface of said second chip, said first attach area having an area substantially equal to the are of said second chip (For Example: See Figure 9); and

Art Unit: 2822

e) a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer (For Example: See Figure 9).

In regards to claims 23 and 28, Derderian discloses the following:

a) first attach layer is a thermosetting material (For Example: See Paragraphs 62 and 63).

In regards to claims 24 and 29, Derderian discloses the following:

a) second attach layer is an inorganic material (For Example: See Paragraph 61).

In regards to claims 25 and 30, Derderian discloses the following:

a) the first and second chips are approximately the same size (For Example: See Figure 9).

In regards to claim 26, Derderian discloses the following:

a) a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface, said first chip mounted on said substrate (For Example: See Figure 9);

b) a wire having a ball bond (For Example: See Figure 9);

c) a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip (For Example: See Figure 9);

d) a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding pads, said first attach layer having an area substantially equal to the area of said second chip (For Example: See Figure 9); and

e) a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer (For Example: See Figure 9).

Art Unit: 2822

Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as obvious over Derderian (U.S. Publication No. 2003/0038355):

In regards to claim 2, Derderian fails to disclose the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10 μm .

However, the applicant has not established the critical nature of the dimension of 10 μm . "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 9, Derderian fails to disclose the following:

a) second attach layer thickness is approximately 1 μm .

However, the applicant has not established the critical nature of the dimension of 1 μm . "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

(10) Response to Argument

APPELLANT'S ARGUMENTS:

1) The Appellant argues that "Derderian does not disclose or suggest the presently claimed invention including a first attached layer to directly couple the first chip and the second chip in the various forms of independent Claims 1 and 21."

2) The Appellant argues that "The Honorable Board's attention is directed to Figure 9 of Derderian where spacers 22 between the layers are shown. The spacers result in a higher profile combination. In contrast the present invention has a low profile."

EXAMINER'S RESPONSE:

1) Merriam-Webster defines the following: a) "directly" as in immediate physical contact; and b) "coupling" as to link. Derderian discloses that "adhesive material 115...may be located between active surface 12 of the first semiconductor device 10 and back side 114 of second semiconductor device 110, securing first and second semiconductor devices 10 and 110 to one another" (For Example: See Paragraph 62). Therefore, the first attach layer (115) does directly couple the first (10) and second chip (110) (For Example: See Figure 9).

2) Derderian discloses the limitations that are disclosed in the claims. There is nothing disclosed in the claims that precludes the utilization of spacers. Therefore, it is not relevant whether Derderian has a high profile and the present invention has a low profile. In addition, the claims do not recite that the claimed multichip module has a low profile.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Art Unit: 2822

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Monica Lewis

Conferees:

Zandra Smith

Drew Dunn

Monica Lewis

Handwritten signatures of the three conferees. Zandra Smith's signature is at the top, Drew Dunn's is in the middle, and Monica Lewis's is at the bottom.

W. Daniel Swayze, Jr.
Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265